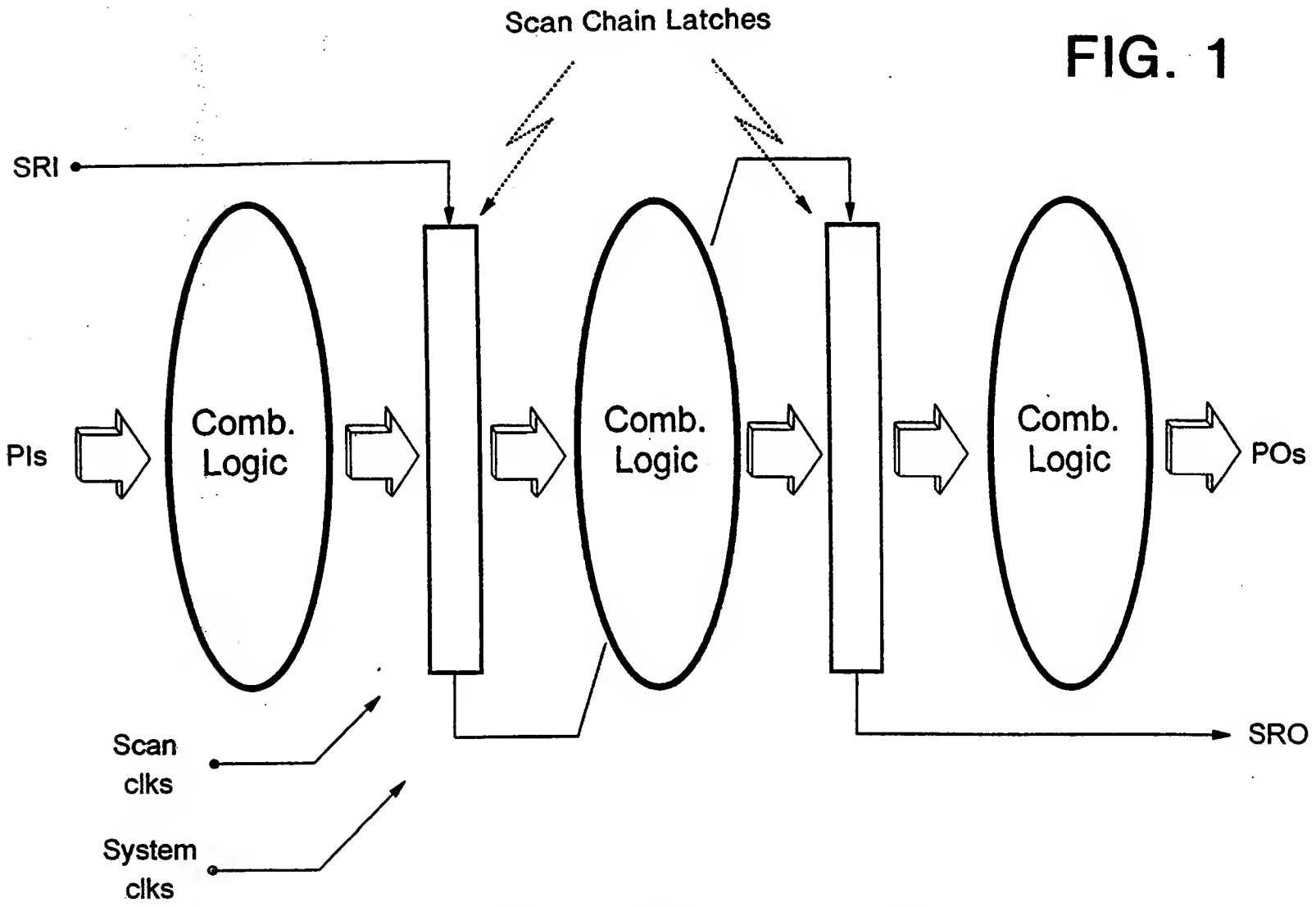
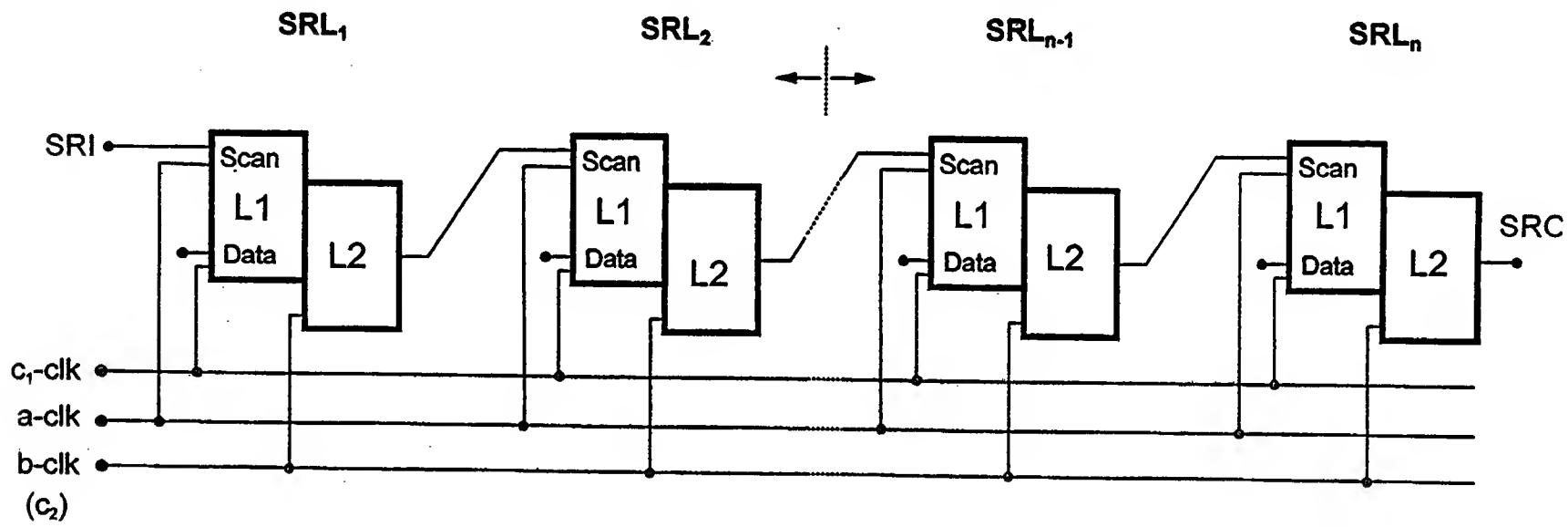
FIG. 1



Typical LSSD Configuration

FIG. 2



Typical LSSD Scan Chain

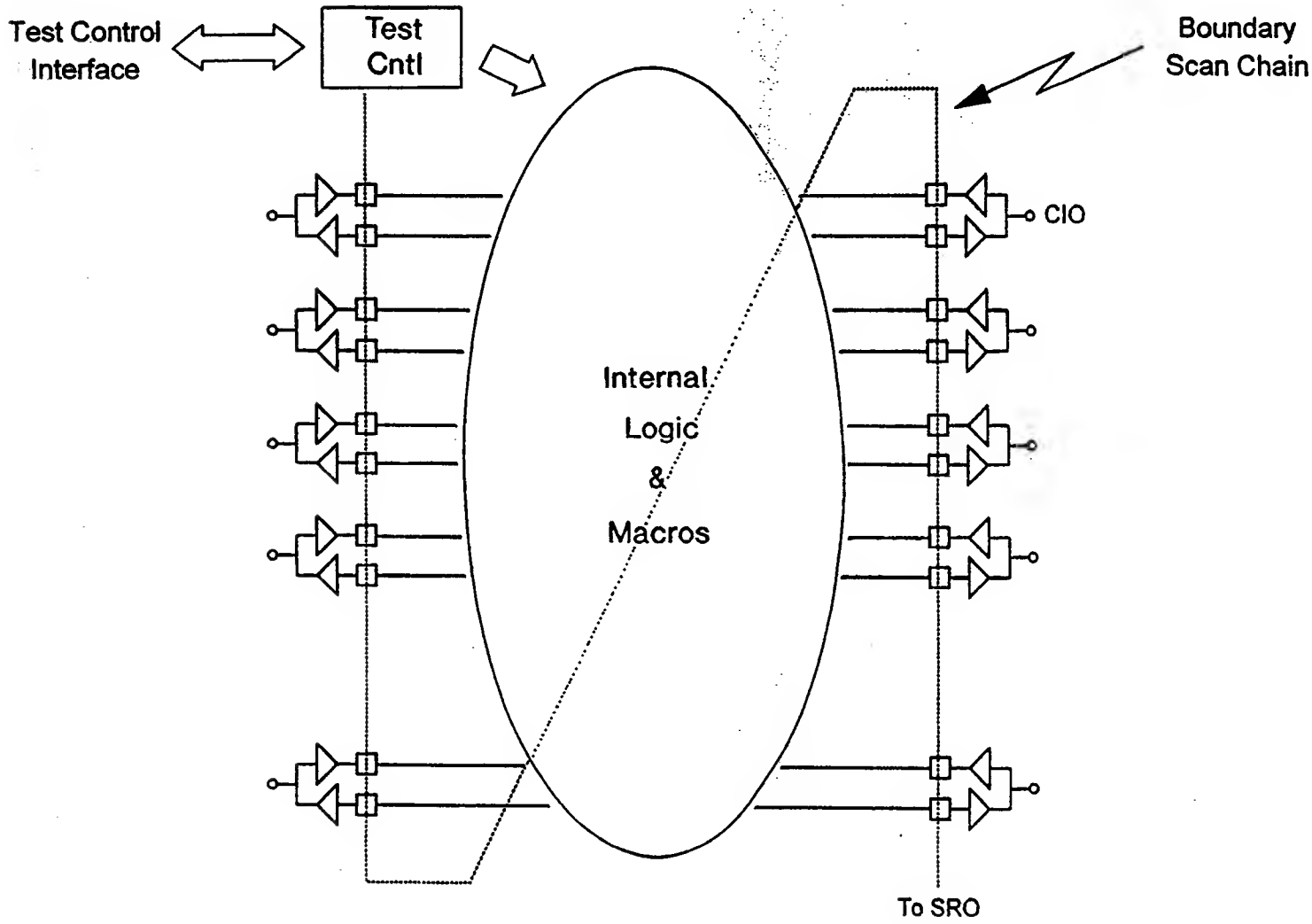
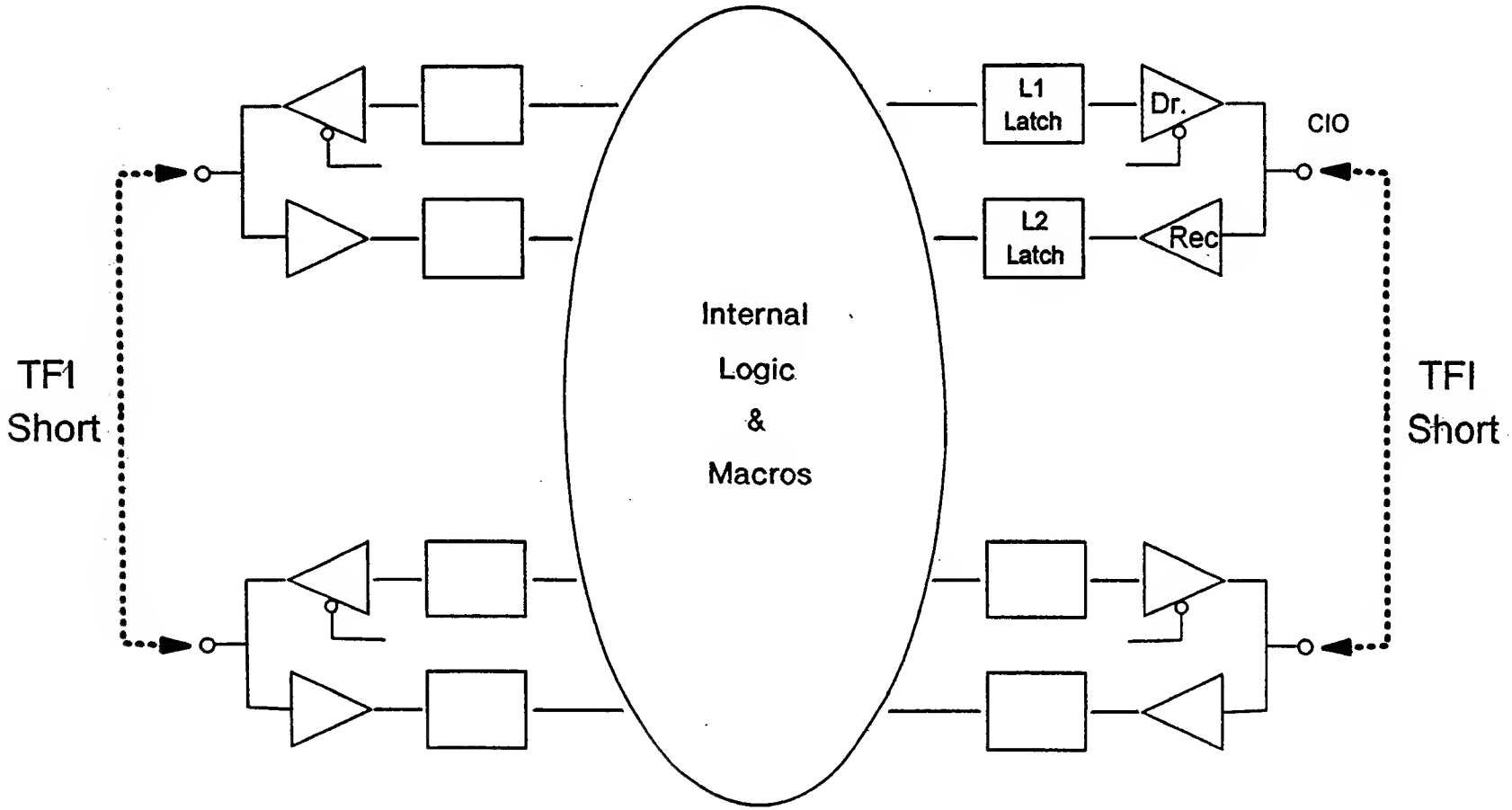


FIG. 3 Boundary Scan Configuration



Typical Common I/O Configuration

FIG. 4

FIG. 5A
Standard

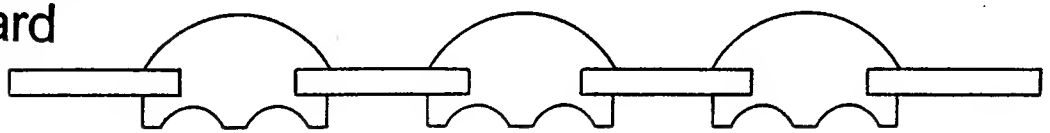


FIG. 5B
Top short

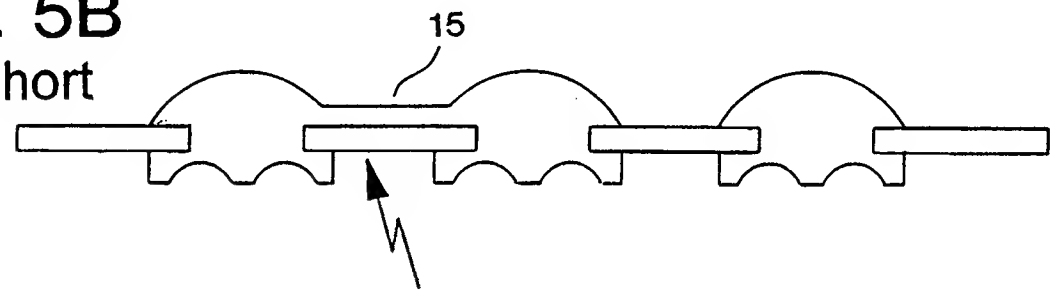
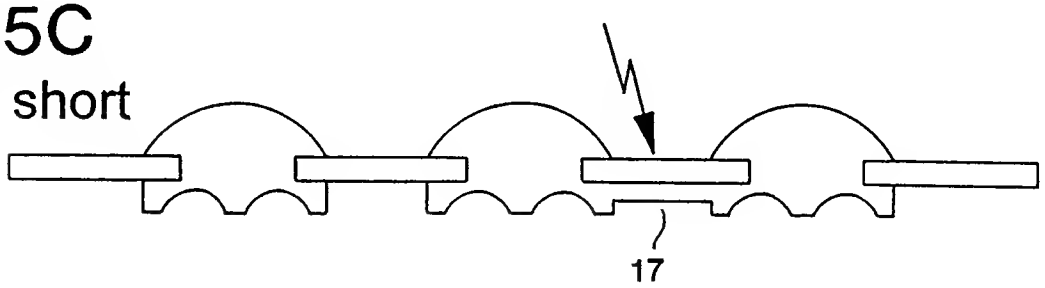


FIG. 5C
Bottom short



TFI Membrane Probe Configurations

FIG. 5D
Starting Material

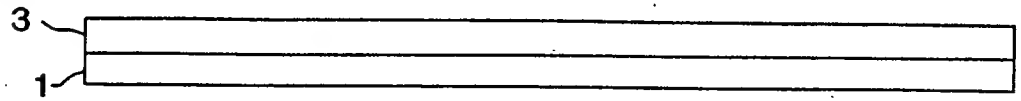


FIG. 6A
Laser Ablate
Blind Vias

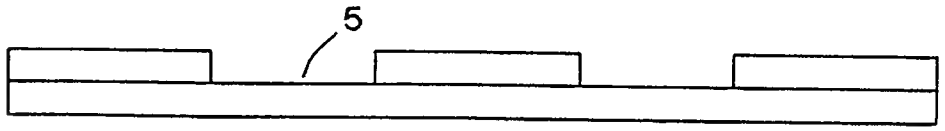


FIG. 6B
Electroplate Copper
in Vias

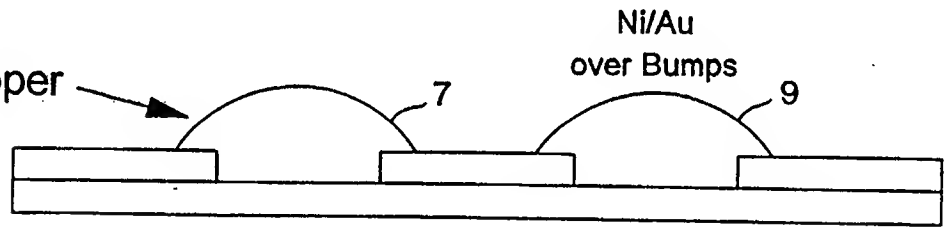
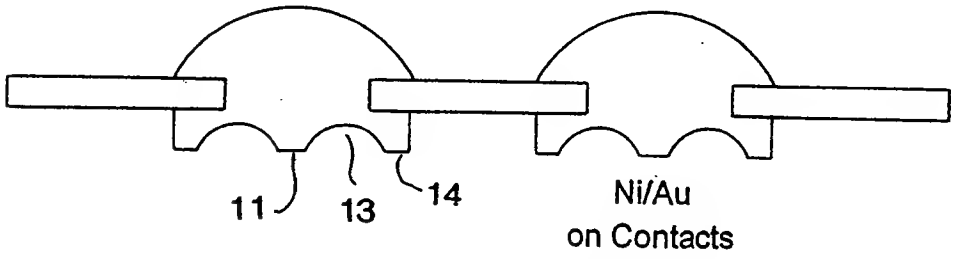


FIG. 6C
Etch Pads
in Copper



Standard TFI Probe Build Process

FIG. 7A
Typical TFI Probe

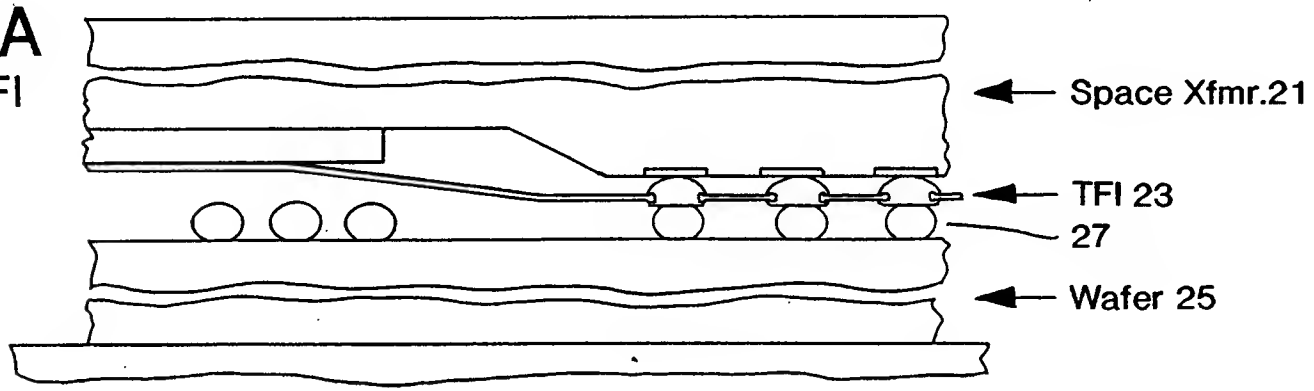


FIG. 7B
TFI Probe with Shorted Pair